Applied Vertical Bloch Line (VBL) Storage Technology

August 11, 1993

Romney R. Katti
Center for Space Microelectronics Technology
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

Presentation Overview

- Technology description review:
  - Functional goals.
  - Performance ranges.
  - VEL operability review.

VBL Technology Functional Performance

Increase reliability:

- Overcome mechanical and environmental limitations.
- Combine nonvolatility and solid-state recorder advantages.

Increase storage capacity and performance:

- Buffer greater quantities of science and engineering data.
- Support onboard computation and processing.
- Simplify data management.
- Provide component with high modularity and storage granularity.
- Increase data transfer rates.
- Provide block access to data.
- Reduce data access times.

Minimize consumption of precious resources:

- Mass, Volume, and Power.

VBL Technology Advantages

VBL technology is the only known storage technology that could fill all of the following requirements simultaneously:

Advantages addressed in proposed development plan:
- Potential near term availability.
- High areal storage density.
- High chip storage capacities.
- High data rate capability.
- Data rate flexibility.
- Low mass, volume, and power consumption.
- Solid-state storage.
- Nonvolatile storage.

Advantages currently considered inherent to VBL technology:
- Radiation hard (SEU and total dose).
- High system capacities.
- High modularity for flexible system design.
- 3D packaging capability for high volumetric storage density.

VBL Applications

Provide compact, high-performance, nonvolatile, solid-state storage for:

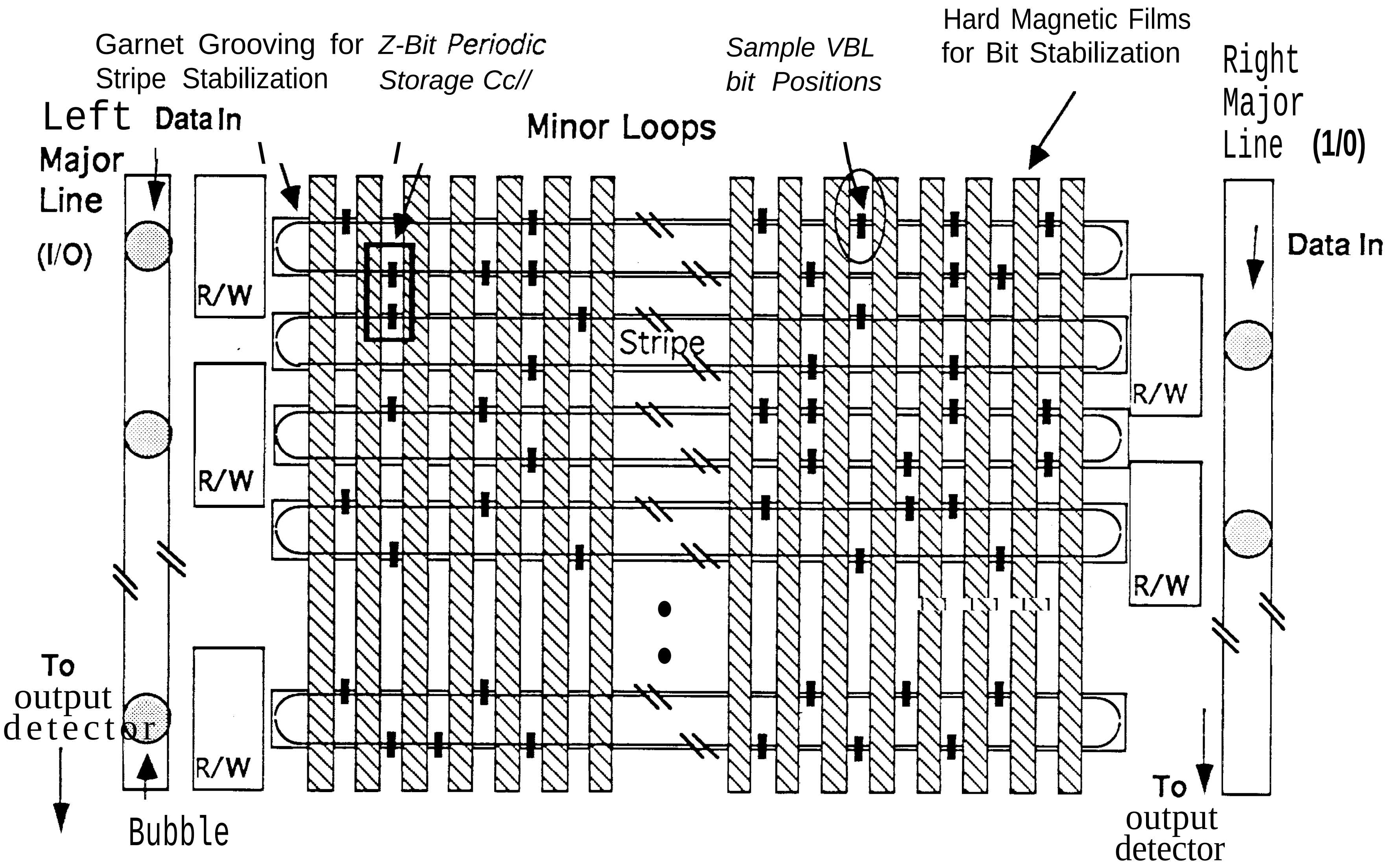
Space applications:

- Microspacecraft.
- Microrovers.
- Planetary spacecraft.
- Earth-orbiting spacecraft.
- Mass storage.
- Embedded subsystem and instrument local storage.
- Distributed multiprocessing and onboard parallel processing.

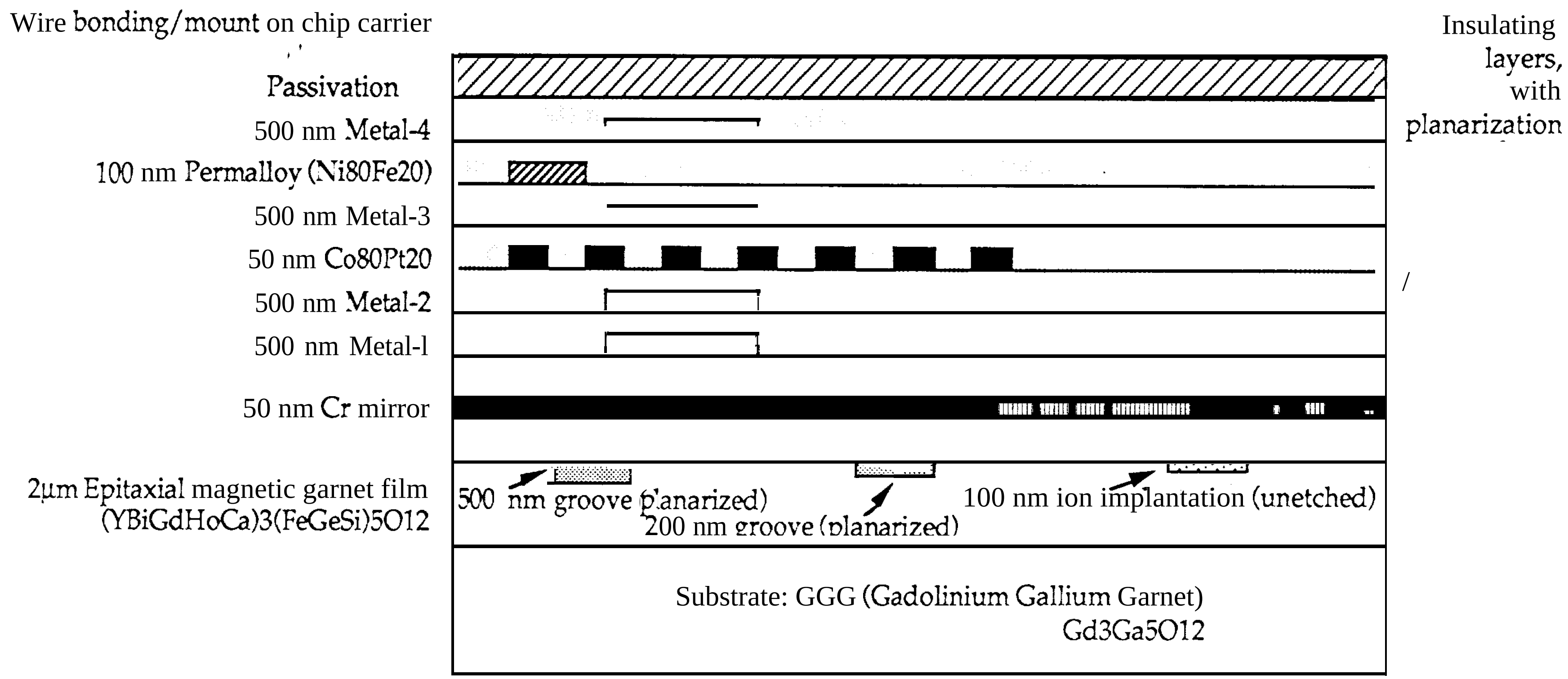
High-volume commercial applications:

- Solid-state disks.
- Laptop and palmtop computer storage.
- Node storage for multiprocessors and supercomputers.

A VBL Memory Architecture



VBL Storage Device Cross-Section



Grooves are formed through ion implantation, and wet etching.
Ion implantation conditions, 1st groove: Ne+, 300 keV, 10^15 ions/cm2.
Ion implantation conditions, 2nd groove: Ne+, 150 keV, 10^15 ions/cm2.
Ion implantation conditions, hard-bubble suppression layer: 80 keV, 10^15 ions/cm2.

Grooves and deposited layers should be planarized.

Layer period is approximately 1 µm.

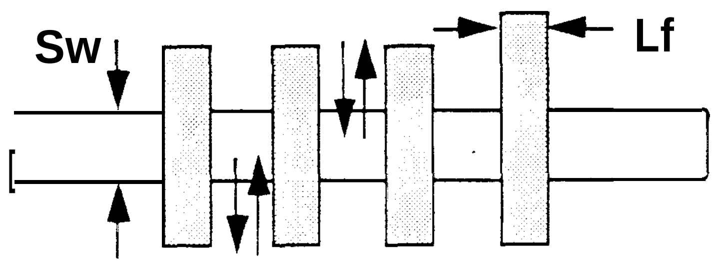
VBL Storage Chips: Areal Storage Density Performance

	Lf = 1 µm	Lf = 0.5 µm	Lf = 0.1 µm
Sw = 5 µm	10 Mbits/cm2	20 Mbits/cm2	100 Mbits/cm2
Sw = 2 µm	25 Mbits/cm2	50 Mbits/cm2	250 Mbits/cm2
Sw = 1 µm	50 Mbits/cm2	100 Mbits/cm2	500 Mbits/cm2
Sw = 0.5 µm	100 Mbits/cm2	200 Mbits/cm2	1,000 Mbits/cm2
Sw = 0.25 µm	200 Mbits/cm2	400 Mbits/cm2	2,000 Mbits/cm2

VBL Memory storage density is proportional to:

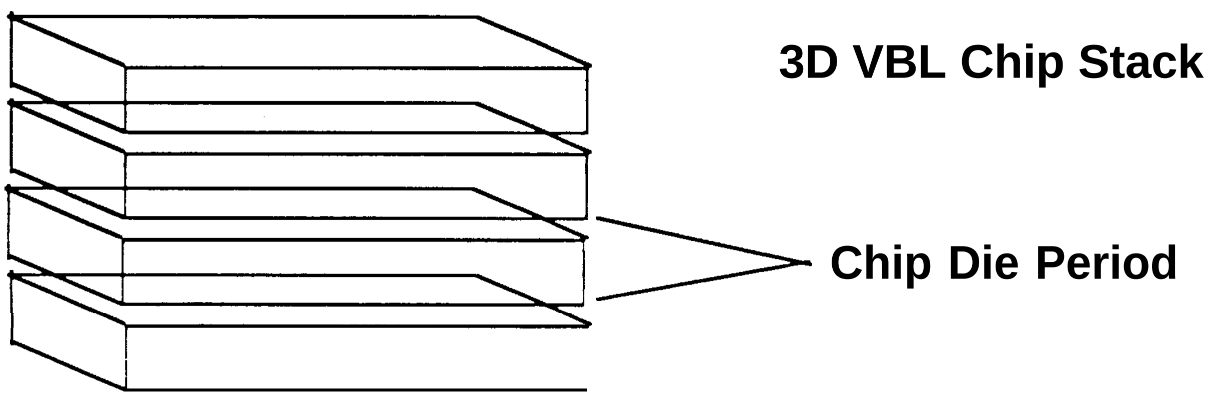
$$\frac{0.5}{(Sw) \times (Lf)}$$

Stripe:



VBL Storage Chips: Volumetric Storage Performance

Areal Storage Density	Chip Die Density: 16 die/cm (25 roils/die) (625 μm/die)	40 die/cm (10 roils/die) (250 urn/die)	200 die/cm (2 roils/die) (50 μm/die)	400 die/cm (1 roil/die) (25 urn/die]
25 Mbits/cm2	0.4 Gbits/cc	1 Gbit/cc	5 Gbits/cc	10 Gbits/cc
100 Mbits/cm2	1.6 Gbits/cc	4 Gbits/cc	20 Gbits/cc	40 Gbits/cc
200 Mbits/cm2	3.2 Gbits/cc	8 Gbits/cc	40 Gbits/cc	80 Gbits/cc
1,000 Mbits/cm2	16 Gbits/cc	40 Gbits/cc	200 Gbits/cc	400 Gbits/cc
10,000 Mbits/cm2	160 Gbits/cc	400 Gbits/cc	2,000 Gbits/cc	4,000 Gbits/cc



VBL Technology
Near Term Development Goals

Solid-state, nonvolatile chips:

16 Mbits, 64 Mbits, and/or 256 Mbit chips.

2 Gbits per cubic centimeter in 3D packaging.

300 Gbits per kg in 3D packaging.

Data rates:

O to >40 Mbit/see per chip.

>1 Gbit/sec per system.

Power consumption:

c 10 mW per Mbit/see during input/output operations.

c 90 mW per active chip during bit propagation operations.

Space qualifiability.

VBL Technology
Longer Term Potential Goals

Solid-state, nonvolatile chips with capacities of:

1 Gbit, 4 Gbits, and greater, are possible.

2 Tbits per cubic centimeter in 3D packaging.

300 Tbits per kg in 3D packaging.

Data rates:

O to >100 Mbit/see per chip.

>1 Gbit/sec per system.

Power consumption:

< 1 mW per Mbit/see during input/output operations.

< 10 mW per active chip during bit propagation operations.

Summary VBL Technology Goals

VBL goals: Improved storage chip performance over DRAMs at disk drive efficiency.

256 Mbit (32 Mbyte) devices	VBL	DRAM	Disk
Solid-state form factor	Yes	Yes	No
Nonmechanical	Yes	Yes	No
Nonvolatile	Yes	No	Yes
Radiation hard medium	Yes	No	Yes
Reduced cost per bit	Yes	No	Yes

V3L Test Device Processing

Phase 2: Test Devices including:

- Two ion implantation steps (with planarization).
- Three metallization steps.
- Two magnetic metal steps.

Test structures provide information on:

- Multimask fabrication in advance of full prototype fabrication.
- Design of full prototype chip (including bias field matching).
- Writing process.
- Read process.
- Bit Propagation.

Test structures will be selected initially from existing design sets.

VML Prototype Device Processing

Phase 3: Full prototype devices including:

- Three ion implantation steps (with planarization).
- Four metallization steps.
- Two magnetic metal steps.

Verify full chip operation on prototype chips.

Include test chips and process verification chips.

Attempt fabrication of a 16 Mbit chip, to assess technical issues.

Prototype devices will be selected primarily from existing design sets.

VBL Testing and Experimentation

Improved electro-magneto-optic sampling microscope has been established to perform key VBL measurements:

- Hardware has been obtained through procurements and loan pool.
- Enhanced computer control with convenient interface.
- Improved image processing to perform quantitative VBL measurements.
- Improved laser operation, fiber-optics, mountings, and couplings.
- High output, fast rise-time electronics have been developed for test flexibility.
- Software programs for creating test chip and full chip test sequences are under development for margin testing.

Continuous illumination microscope is in place for complementary magnetic measurements.

Laboratory space is likely to support experimentation and simulation activities.

- VBL domain simulations will move from SUN SPARC 2GX platform to IBM-compatible 80486-based PC with doubling of throughput.

VBL Dynamics Research

Dr. Anne Bagneres, JPL visiting scientist, is continuing her interaction with JPL using the 512-node Caltech Intel Touchstone Delta:

- Demonstrated demagnetizing field calculation.
- Demonstrated improved demagnetizing field calculation.
- Working towards implementing entire micromagnetic VBL simulation on the Delta.

Contract to Boston University (BU) has been extended through May, 1993.

Research at BU continues on the subjects of:

- Experimental VBL dynamics.
- Supercomputer simulations on the CM-5.

VBL Dynamics Research-2

Dr. Anne Bagneres, JPL visiting scientist, is continuing her interaction with JPL using the 512-node Caltech Intel Touchstone Delta:

- Working towards implementing entire micromagnetic VBL simulation on the Delta, July, 1993.

Contract to Boston University (BU) has been extended through May, 1993. Research at BU continues on the subjects of:

- Experimental VBL dynamics.
- Supercomputer VBL simulations on the CM-5.

CM-5 accessibility:

- Assessing access to JPL SAR project's CM-5 in Bldg. 300.
- Assessing access to CM-5 at NASA Ames.

Conclusions

VBL storage technology offers many excellent data storage technology attributes.

VBL technology is multidisciplinary in nature and is best served through the involvement of many organizations.

VBL fabrication is proceeding under a phased plan to fabricate full prototype VBL chips by 2Q, FY'94.

VBL laboratory is being improved to perform precise measurements of VBL performance, to evaluate forthcoming VBL chips.

Supplemental Slides

VBL Chip Cost Competitiveness

Assume $5 K/wafer (processing + wafers+ material) (Overestimate)
Assume 50 chips are yielded per wafer (Underestimate)
Therefore chip cost is $1 00/chip.
For a 256 Mbit chip (32 Mbyte), cost is $3/Mbyte.

VBL bit costs are thus less costly than DRAM bit costs by an order of magnitude.

VBL bit costs are therefore comparable to magnetic disk drive bit costs.

VBL capitalization is estimated at $10M, which is less than $1 OOM for a DRAM line.

It is noted that VBLdevices have implants, deposition, and lithography, but, unlike DRAMs (and SRAMs) have no diffusions and very few contacts.

VBL devices are therefore much simpler to process than DRAMs.

VBL technology offers very desirable price/performance ratios.

JPL V3L Staff

R. Katti, Lead Technologist
U. Lieneweg, Design and process control
D. Opalsky, Instrumentation and experimentation
G. Patterson, Simulation

Honeywell Corp., Fabrication
Boston University, Research
A. Bagneres, Visiting Scientist, Simulations
G. Tardio, Wafer Testing
Visiting Industrial Fellows